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Checking ESD path resistance in IC designs

Design to Silicon

Finding and eliminating ESD issues is critical to ensuring the reliability of IC chip designs. The Calibre PERC reliability platform provides a complete, automated solution for quickly and accurately detecting and debugging P2P resistance violations and bottlenecks in ESD paths, enabling designers to deliver even the largest and most complex IC designs on schedule without compromising performance reliability.

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Introduction

With growing die sizes and increasing transistor densities in integrated circuit (IC) chip designs, the verification and debugging of electrostatic discharge (ESD) issues have become both more critical and more challenging [1, 2]. Not only does verification require more computing resources (such as CPUs, memories, and runtimes), but the debugging of ESD violations is also becoming more difficult, due to the complexity of today's large IC designs.

To ensure sufficient protection against an ESD event, IC designers must make sure that not only are ESD protection devices implemented, but also that the ESD discharge paths are efficient and robust. For example, a rule that is often included in rule decks is that the resistance of an ESD discharge path, which is the path between an ESD source (e.g., a physical pad) and its ESD protection device, must be less than a certain design threshold [2].

Finding and debugging ESD protection violations can be difficult and time-consuming. Fortunately, layout designers can use the Calibre® PERC™ reliability platform in conjunction with the Calibre RVE™ results viewer and Calibre DESIGNrev layout viewer to quickly and automatically check the resistances of ESD discharge paths in an IC layout design, and identify any problematic layouts (i.e., resistance bottlenecks) that require fixing.

Figure 1 illustrates some typical ESD protection schemes and common ESD discharge paths [3-4]. In figure 1a-d, the I/O pad is protected by pull-up and pull-down diodes, an ESD resistor, and secondary ESD diodes. A power clamp is connected between the power bus VDD and ground bus VSS. In figure 1e, a pair of back-to-back connected diodes are used to connect the ground busses VSSA and VSSB from two power domains.

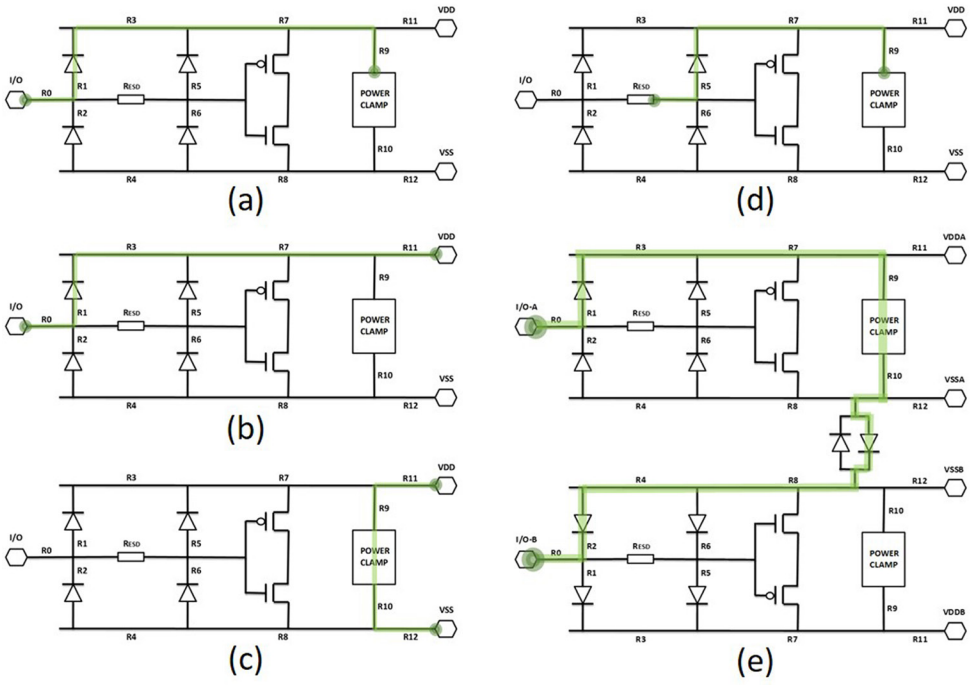

Figure 1: Common ESD protection schemes and ESD discharge paths (highlighted in green): (a) I/O pad and power clamp; (b) I/O pad and power pad; (c) power pad and ground pad; (d) ESD resistor and power clamp; (e) I/O pad and I/O pad [3, 4].

Maximum allowed point-to-point (P2P) resistance values along ESD discharge paths are critical constraints in ESD protection schemes. Calculating these values requires topology information from the layout design, such as ESD devices (e.g., pull-up and pull-down diodes, power clamps, etc.), as well as the locations of I/O, power and ground pads, etc.

The Calibre PERC P2P resistance flow first runs layout extraction on the input layout database, based on layout vs. schematic (LVS) rule decks. Using the resulting layout netlist, the Calibre PERC tool runs topology analysis to identify I/O, power and ground pads, ESD devices such as pull-up and pull-down diodes, and power clamps, etc. Different ESD discharge paths can be defined in the rule decks.

The Calibre PERC platform then runs simulation to determine the effective resistances along the ESD discharge paths. The calculated resistance values are compared to the design thresholds, which are set based on the process technology, and defined in rule decks. All violations are output to a results database, which is viewed and debugged using the Calibre RVE results viewer.

Let's use a simple design case to demonstrate how to use the Calibre PERC and Calibre RVE tools to check the resistances along ESD discharge paths and debug resistance violations.

Checking ESD path resistances

Figure 2 shows a simple circuit design in which an I/O pad named "INA" should be protected by pull-up and pull-down diodes. Figure 2a is the schematic, showing an I/O pad "INA" connected to a pull-up and a pull-down diode, and Figure 2b is the corresponding layout design. In Figure 2c, resistance between the I/O pad "INA" and the pull-down diode is displayed as a violation in Calibre RVE results viewer, with 2d using the Calibre DESIGNrev layout viewer to display a fly-line highlighting the resistance violation between the I/O pad "INA" and the pull-down diode.

To ensure sufficient ESD protection on the I/O pad "INA", designers must not only ensure that the pull-up and pull-down diodes are connected to the I/O pad and meet certain dimension requirements, but also ensure that the resistance between the I/O pad "INA" and the pull-up or the pull-down diode, respectively, is within the design threshold.

Most semiconductor foundries provide their customers with foundry-supported Calibre PERC flows to check for ESD protections in layout designs that will be manufactured by those foundries. This eliminates the need for a design company to write its own Calibre PERC rule decks to check for common ESD rules, although they may choose to write custom Calibre PERC decks to check for their own unique ESD requirements.

The Calibre PERC platform is seamlessly integrated with Calibre LVS rule decks. A Calibre PERC flow for checking resistances along ESD paths first runs layout extraction based on the LVS rule deck to generate the device and connectivity information of a layout design. Based on definitions given in rule decks, it then determines the source and sink (or pin pair) for resistance calculation (in figure 2, this is the I/O pad "INA", and the pull-up or pull-down diode, respectively). The Calibre PERC platform calculates the total effective resistance between a pin pair using simulation. Any pin pair with a total effective resistance value higher than a pre-defined design threshold is flagged as a violation. In the simple design shown in figure 2, the resistance between the I/O pad "INA" and the pull-down diode is approximately 15.8 ohms, which exceeds the given design threshold of 2.0 ohms. This measurement is flagged as a resistance violation.

After loading the results in the Calibre RVE results viewer, designers can see the resistance violation is flagged, as shown in figure 2c. Highlighting this resistance violation in Calibre RVE enables designers to use the Calibre DESIGNrev layout viewer to display a fly line between the source (I/O pad "INA"), and the sink, which is the pull-down diode, as shown in figure 2d.

In a large and complex layout design, however, merely knowing there is a resistance violation on an ESD discharge path does not give layout designers enough information to fix the violation. Layout designers must be able to determine where in the layout they must make changes to reduce the resistance of the ESD path. Let's look at how layout designers can quickly and accurately debug a resistance violation using the Calibre RVE results viewer and Calibre DESIGNrev layout viewer.

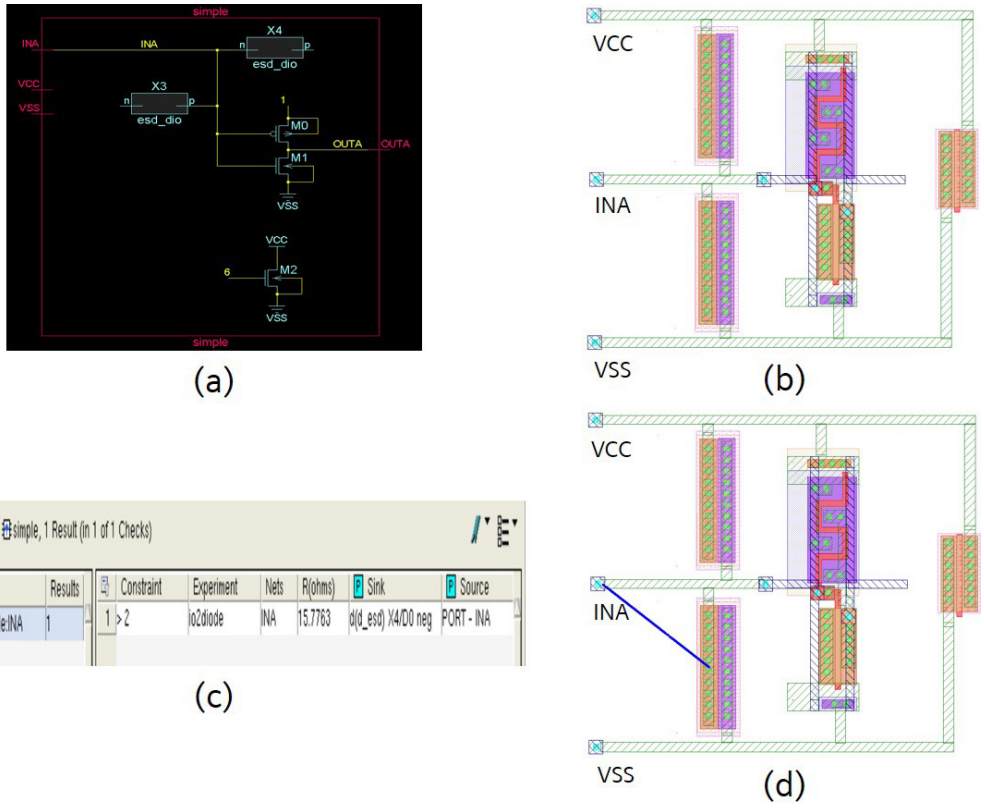

Figure 2: ESD protection verification and error detection in a simple circuit design with ESD protection on I/O pad.

Debugging resistance bottlenecks

The Calibre PERC platform generates debug information that can be used to highlight an entire ESD path containing resistance violation. Using the Calibre DESIGNrev layout viewer, designers can highlight all polygons on an ESD path, including metal routes and vias, that contribute to the total effective resistance exceeding a given design threshold, as shown in figure 3a.

The Calibre PERC flow also reports information such as the percentage contribution of each metal and via polygon to the total effective resistance of an ESD path. By initiating the Calibre DESIGNrev colormap feature in the Calibre RVE results viewer, layout designers can highlight the metal and via polygon segments of an ESD path, using different colors based on each polygon's percentage contribution to the total effective resistance. In figure 3b, the polygon segments of the ESD discharge path between the I/O pad "INA" and the pull-down diode are highlighted in different colors, with red indicating the highest percentage contributions, and blue the lowest percentage contributions. The percentage range of each color is shown in the layout viewer, and can be adjusted to suit the preference of each user. The polygon segments with highest percentage contributions to the total effective resistance are usually the resistance bottlenecks on the ESD path. This highlight capability provides a useful visual aid to layout designers when tracing an ESD path for possible layout issues and fixes, especially in a large and complex layout design (such as a full chip layout database).

This colormap feature allows layout designers to quickly identify the resistance bottlenecks along an ESD path, and make necessary layout changes, such as widening metal routes or adding additional vias, to reduce the total effective resistance of the ESD path. This debug feature of Calibre tools has proven to be especially helpful when debugging resistance violations in a large and complex layout design, where manually inspecting the layout for resistance bottlenecks is extremely difficult and time-consuming.

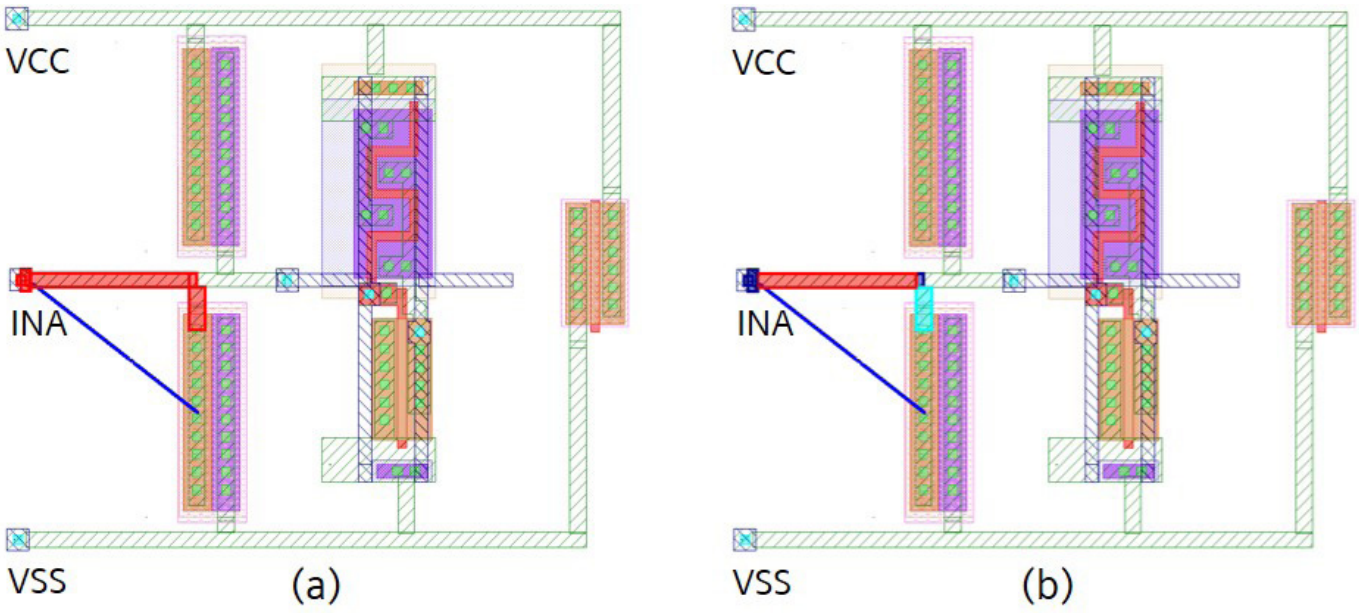

Figure 3: Debugging resistance violation of an ESD path in a simple circuit design with ESD protection on I/O pad. (a) All polygon segments with a resistance violation are highlighted in red; (b) Polygon segments with a resistance violation are highlighted in different colors based on the percentage contribution of each polygon to the total effective resistance of the ESD path.

Conclusion

With advanced semiconductor process nodes, and the smaller transistor and interconnect feature sizes in today's IC designs, finding and eliminating ESD problems is becoming more critical to ensuring the reliability of IC chip designs. Checking the resistances of ESD discharge paths in a layout, and determining if they are within pre-defined design thresholds, plays an important role in meeting the requirements of ESD protection in IC chip designs. The Calibre PERC reliability platform provides a complete solution for checking a layout design for resistance violations along ESD paths, highlighting resistance violations for faster and easier debugging, and identifying resistance bottlenecks for layout fixes. The Calibre PERC reliability platform helps designers alleviate the difficulties of detecting and debugging ESD issues in today's large and complex IC chip designs.

References

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